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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 20

Application Number	10/027,978
Filing Date	October 24, 2001
First Named Inventor	Michael W. Morrow
Art Unit	2188
Examiner Name	Tran, Denise
Attorney Docket Number	42390.P12943

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
- [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Intel Corporation		
Signature			
Printed name	Stuart A. Whittington		
Date	December 22, 2005	Reg. No.	46,215

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Typed or printed name	Stuart A. Whittington	Date	12/22/05

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($)	500

Complete if Known	
Application Number	10/027,978
Filing Date	October 24, 2001
First Named Inventor	Michael W. Morrow
Examiner Name	Denise Tran
Art Unit	2185
Attorney Docket No.	42390.P12943

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 50-0221 Deposit Account Name: Intel Corporation

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fee ($)	Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____ x	_____	= _____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____ x	_____	= _____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number)	x _____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief -Fee Code: 1402	$500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 48,215	Telephone 480-715-3696
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I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING FACSIMILE TRANSMITTED TO THE U.S. PATENT AND TRADEMARK OFFICE (FAX NO. (571) 273-8300), ON THE DATE INDICATED BELOW:

Date of Transmission: 12/22/05 By: Stuart Whittington

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Michael W. Morrow

Atty. Docket No: 42390.P12943

Appln. No.: 10/027,978

Group Art Unit: 2185

Filed: October 24, 2001

Examiner: Tran, Denise

Title: APPARATUS AND METHOD TO PERFORM ADDRESS TRANSLATION

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

Pursuant to Appellant's Notice of Appeal filed on November 3, 2005, Appellant presents this Brief in appeal of the Final Rejection dated June 3, 2005.

I. REAL PARTY IN INTEREST.

Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES.

There are no related appeals or interferences before the Board of Patent Appeals and Interferences or related judicial proceedings known to Appellant, the Appellant's legal representatives, or assignee that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

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III. STATUS OF CLAIMS.

Claims 1-33 have at one time, been pending in the present application. Claims 1-13 and 29-33 were cancelled due to restriction and thus only claims 13-28 remain pending. Claims 13-28 stand finally rejected and are the claims subject to this appeal, which are reproduced in attached Appendix A.

IV. STATUS OF AMENDMENTS.

An after final amendment was submitted by Appellant on September 8, 2005 which only presented amendments to the Abstract to address certain objections. The Advisory Action dated November 1, 2005 indicated the amendment would be entered into the record.

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Embodiments of the instant invention relate to microprocessor systems that use virtual memory addressing. One problem that may arise with systems that use conventional memory management unit (MMU) configurations is that the address translations and memory protection operations performed by MMUs may be time consuming relative to other operations of the system. (Specification, pg. 2, ll. 9-15). Most notably, in conventional MMU configurations, access to the physical memory and/or memory controller by an MMU may be constrained by a multiplexer or other interface and thus performing a table walk (a process of translating virtual address into physical memory addresses or visa versa) requires that requests from the MMU (and replies for the memory) travel through several levels of logic/flip-flops and often a clock domain.

Embodiments of Appellant's invention may eliminate much of this latency by moving table walk logic closer to the memory. By way of example, referring to Appellant's Fig. 1, a computing system 110 may include a processor 120, a multiplexer (MUX) 130 connected to the processor 120, a translation lookaside buffer (TLB) 140 connected to the processor 120 and a MMU 150 connected to the TLB 140. Additionally, system 110 may include a memory controller 160 connected to MUX 130, a table walk device 170 connected to memory controller 160 and a memory device 190 connected to memory controller 160. (Spec. pg. 4, ll. 21 - pg. 5, ll. 4).

In one embodiment, memory controller 160 and table walk device 170 may be combined as a bus controller 195. (Spec. pg. 5, ll. 4-6). Memory controller 160 may control memory 190 by providing read and write signals or refresh signals (e.g., if memory 190 is a volatile memory device) or control programming or erasing (e.g., if memory 190 is a nonvolatile memory device). (Spec. pg. 7, ll. 4-11). Table walk device 170 may be adapted to perform a table walk operation that may include retrieving information from translation tables stored in memory 190. Entries in the tables may be used by table walk device 170 to perform virtual-to-physical address translations. (Spec. pg. 7, ll. 19-24).

Conventionally, table walk logic is located within an MMU or processor with the MMU. However, according to aspects of Appellant's embodiments (e.g., claim 14 and 23), a table walk device 170 is moved outside the clock domain of the MMU and is provided on the same clock

domain of the memory controller 160 to reduce latencies associated with conventional memory controller accesses via a MUX or other interface (Spec. pg. 10, ll. 19-22).

In various embodiments, table walk device 170 may comprise a table base register to store a table base address (claim 16; Spec. pg. 9, ll. 17-18) and/or be adapted to provide descriptors to TLB 140 (claim 18). Table walk device may also receive memory access protection data (claim 19) and provide memory access protection by determining wither a process executing in processor 120 is permitted to access data stored in memory 190. (Spec. pg. 7, ll. 23 to pg. 8, ll. 1-5 and pg. 10, ll. 9-15). MMU 150 may be adapted to perform part or all of the memory access protection. For example, after a table walk is performed by table walk device 170, the information derived from the table walk may be transmitted to MMU 150. (Spec. pg. 8, ll. 23 to pg. 9, ll. 1.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.

The issues for consideration on this Appeal are:

A. Whether claims 14-28 are properly rejected under 35 U.S.C. § 112, first paragraph, as failing to disclose the best mode contemplated by the inventor;

B. Whether claims 23-24 and 26-28 are properly rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6, 681,311 to Gaskins et al. (hereinafter "Gaskins");

C. Whether claims 14, 17 and 20 are properly rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,658,538 to Arimilli et al. (hereinafter "Arimilli");

D. Whether claims 14-18 and 20 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,666,509 to McCarthy et al. (hereinafter "McCarthy") in view of U.S. Patent 5,937,437 to Roth et al. (hereinafter "Roth");

E. Whether claims 19, 21 and 22 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over McCarthy in view of Roth in further view of U.S. Patent 4,766,537 to Zolnowsky;

F. Whether claim 25 is properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaskins in view of McCarthy;

G. Whether claims 15, 16 and 18 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli in view of McCarthy; and

H. Whether claims 19 and 21-22 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli in view of Zolnowsky.

VII. ARGUMENT.

A. APPELLANT'S APPLICATION COMPLIES WITH THE "BEST MODE" REQUIREMENT OF 35 U.S.C. § 112 FIRST PARAGRAPH.

The Office Action has taken the position that Appellant's frequent use of the terms "may be" or "may" in describing the preferred embodiments, equates to a concealment of the best mode. Appellant respectfully notes that "[t]here is no requirement in the statute that applicants point out which of their embodiments they consider to be their best; that the disclosure includes the best mode contemplated by applicants is enough to satisfy the statute." *Ernsthausen v.*

Nakayama, 1 USPQ2d 1539 (Bd. Pat. App. & Inter. 1985) (emphasis added). Further, an examiner should assume that the best mode is disclosed in the application, unless evidence is present that is inconsistent with that assumption. See, MPEP 2165.03.

In the instant case, the Examiner has not even alleged that the best mode is not disclosed in the application, only that Appellant has not specifically identified which potential variations are considered to be the best mode in the application. Accordingly, Appellant respectfully submits that the present rejection is improper on its face since no evidence or arguments have ever been presented that Appellant's specification does not describe the best mode known to the inventor at the time the application was filed. Accordingly, Appellant respectfully requests the Board to overturn this §112 first paragraph rejection.

B-C. APPELLANT'S CLAIMS ARE NOT ANTICIPATED BY EITHER GASKINS OR ARIMILLI.

Prima facie anticipation under 35 U.S.C. § 102 is established only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Veregall Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

In the case at hand, Appellant respectfully submits that neither Gaskins nor Arimilli disclose or suggest each and every feature of respective claims 14, 17, 20 or 23-24 and 26-28.

B. Gaskins

Gaskins discloses an apparatus and method for caching memory types in the lookaside buffer (TLB) of a processor in order to reduce the time required to obtain the memory type.

Col. 3, ll. 14-19. The Final rejection alleges that the limitation of Appellant's independent claim 23 which recites "*a discrete memory controller adapted to perform a table walk operation,*" is disclosed by Gaskins as element 106 (Fig. 7).

Respectfully, Appellant believes the Examiner has incorrectly interpreted Gaskins table walk logic element 106 as being analogous to Appellant's claimed discrete memory controller by alleging "[a]pplicant has failed to show any other functionality performed by the discrete memory controller other than table walk functions." (6/3/05 Office Action pg. 14). Appellant respectfully believes the Examiner has improperly overlooked how the skilled artisan would interpret Appellant's claimed discrete "memory controller," particularly when read in light of Appellant's specification as well as the cited references of record. Table walk logic 106 of Gaskins is part of a processor data unit 700 (col. 9, ll. 30-36) and thus suffers from the latency problems of accesses through MUXs 104, 704 that Appellant's embodiments are intended to reduce. Gaskins data unit 700 and/or its associated table walk logic 106 is not a discrete memory controller adapted to perform table walks as claimed in Appellant's claim 23. In fact, Gaskins explicitly teaches that, data unit 700 interfaces with a separate memory controller using processor bus 148. (Col. 4, ll. 60-66).

Because Gaskins fails to teach or suggest at least *a discrete memory controller adapted to perform a table walk operation*, and in fact teaches away from this limitation by including table logic 106 in the processor itself, Gaskins cannot anticipate claim 23 or claims 24 and 26-28 which depend there from.

C. Arimilli

Arimilli discloses a non-uniform memory access (NUMA) data processing system having a page table including node-specific control bits. A plurality of nodes contain a plurality of processing units and at least one system memory having a table (e.g., a page table) resident therein. The page table includes at least one entry for translating a group of virtual addresses to physical addresses that individually specify control information pertaining to the group of virtual addresses for each of the plurality of nodes. (Col. 3, ll. 11-20). It is worthy of noting that the page table does not perform any address translation, it only stores known virtual to physical address correlations.

As shown by Fig. 1, Arimilli discloses a system 10 that includes two or more processor nodes 12. Each node includes one or more processing units 14 which include a CPU 20 (Fig. 2) and a memory controller 24 separate from CPU 20 that controls access to an associated one of the physical system memories 26. (Col. 4, ll. 14-38.) As plainly shown by Arimilli, CPU 20 includes a data memory management unit (DMMU) 48 and an instruction memory management unit (IMMU) 50 to respectively translate addresses of data and instructions into virtual addresses and then into physical addresses (col. 8, ll. 1-6) and performs page table search operations using tablewalk controller 78. Thus Arimilli makes clear that tablewalk controller 78 and memory management units 48, 50 are both included in the same CPU unit 20 and not in direct physical connection with memory controller 24 (Fig. 2).

Accordingly, Appellant respectfully submits that Arimilli fails to teach or suggest *a table walk device connected to the memory controller and externally located from a memory management unit* as recited in Appellant's claim 14. (See Appellant's specification pg. 4, ll. 1-6 for proper interpretation of "connected to"). In fact, Arimilli expressly teaches away from the foregoing limitations of Appellant's claim. Because Arimilli fails to teach or suggest at least the foregoing feature of Appellant's claim 14, Arimilli do not anticipate claim 14 or the claims which depend there from (including claims 17 and 20).

In view of the foregoing, Appellant respectfully requests the Board to overturn to the §102 rejections of record based on Gaskins and Arimilli.

D-H. APPELLANT'S CLAIMS ARE NOT RENDERED UNPATENTABLE BY THE COMBINATIONS OF: (D) McCARTHY IN VIEW OF ROTH AND/OR (E) IN FURTHER VIEW OF ZOLNOWSKY; (F) GASKINS IN VIEW OF McCARTHY; (G)ARMILLI IN VIEW OF McCARTHY; OR (H) ARIMILLI IN VIEW OF ZOLNOWSKY.

LEGAL STANDARD

It is well established that *prima facie* obviousness is only established when three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991) (MPEP 2144).

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary sill in the art. *In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

ARGUMENT

In the instant case Appellant respectfully submits that, (1) there is no proper motivation to combine the references as suggested, and (2) even when combining the combining the cited references as proposed, the resultant combinations still fail to teach or suggest several features of Appellant's claims.

D. Claims 14-18 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McCarthy in view of Roth. The rejection alleges that McCarthy discloses all of the limitations of independent clam 14 with the exception of a table walk device externally located from an MMU and relies on Roth to make up for this deficiency alleging it would be obvious to combine McCarthy with Roth to "provide for parallel operation of the data and instruction caches. By having a DMMU and a IMMU in McCarthy two MMUs would be present where each table walk controller would be separate from the other MMU." (6/3/05 Final Office Action pg. 9).

McCarthy discloses a processor 10 having a data cache unit 16 wherein the data cache unit includes an MMU 32. The MMU 32 (Fig. 3) contains a table walk controller 42 to perform virtual address translations. (Col. 4, ll. 42-45). Thus McCarthy explicity teaches away from a table walk controller which is externally located from an MMU as recited in Appellant's claim 14.

Roth discloses a method and apparatus for performance monitoring of virtual memory address translation. (Col. 2, ll. 31-34). Processor 100 is a single integrated circuit and includes performance monitoring hardware (PMH) 140 and instruction and data MMUs 124, 134 which include logic/registers/caches to perform virtual address translation. (Col. 3, ll. 44-66).

(1) To the extent Appellant can comprehend the proposed motivation for combining these references (e.g., to provide for parallel operation of data and instruction caches), it appears that Roth may be able to perform this in and of itself. Thus there appears to be no benefit for the skilled artisan to entirely redesign and reconstruct the device of McCarthy when the device of Roth already performs parallel operation of data and instruction caches. Accordingly, there is no proper objective reason for the skilled artisan to combine references as suggested in the Office Action and *prima facie* obviousness is not established.

(2) Moreover, even assuming it would be proper to combine McCarthy and Roth as proposed (*arguendo*), Appellant respectfully submits the resultant combination would still fail to teach or suggest the limitation of *a table walk controller connected to the memory controller and externally located from an MMU* as recited in Appellant's claim 14. For the foregoing reasons

Appellant respectfully submits *prima facie* obviousness has not been established and respectfully requests the Board to overturn the §103 rejection based on the combination of McCarthy and Roth.

E. Claims 19, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over McCarthy in view of Roth in further view of Zolnowsky. The rejection alleges the combination of McCarthy and Roth disclose the features of these claims with the exception of the use of a *table walk device adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device* or *abort a signal to the processor if the process is not permitted access to the memory device*. The rejection relies on Zolnowsky to make up for these deficiencies.

Ignoring the properness of the motivation to combine Zolnowsky with the combination of McCarthy and Roth, Appellant respectfully submits that because the combination of McCarthy and Roth fails to establish *prima facie* obviousness with respect to independent claim 14 (discussed in D above), the claim from with claims 19, 21 and 22 depend, and because Zolnowsky fails to remedy the deficiencies of the proposed combination of McCarthy and Roth (i.e., improper motivation to combine and all limitations of claim 14 are not disclosed by the combination), Appellant submits this cited combination also fails to establish *prima facie* obviousness for at least the same reasons. Accordingly, Appellant respectfully requests the Board to overturn the §103 rejection based on the combination of McCarthy, Roth and Zolnowsky.

F. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Gaskins in view of McCarthy. The rejection alleges that Gaskins discloses all of the subject matter of this claim with the exception of *providing memory access protection by preventing a process in the processor from accessing predetermined data in the volatile memory device*, and relies on McCarthy to make up for this deficiency. The rejection alleges it would be obvious for the skilled artisan to combine McCarthy with Gaskins to "provide for protection against unauthorized access at the earliest stage of address processing." (6/3/05 Final Office Action pg. 11).

(1) Appellant respectfully submits that McCarthy in fact does not disclose *providing memory access protection by preventing a process executing in the processor from accessing data in the nonvolatile memory device* as alleged. Rather the cited portion of McCarthy (col. 5, ll. 17-20) relates to restrictions for write access, as opposed to read access, for an ATC entry. Additionally, once again the Office Action is alleging a first reference (Gaskins) should be modified to have the benefits of a second reference (McCarthy) but does not explain why the skilled artisan would bother entirely redesigning and reconstructing the first reference when it appears the second reference alone provides the desired functionality. Thus it appears that the only motivation to combine references is derived in a piecemeal attempt to reconstruct Appellant's claims based on the improper hindsight of Appellant's disclosure. Consequently, the motivation to combine references appears flawed and *prima facie* obviousness has not been established for this reason alone.

(2) Appellant further submits that Gaskins fails to teach or suggest the limitations, namely *a discrete memory controller adapted to perform a table walk operation*, of independent claim 23 (from which claim 25 depends) as discussed previously (Section B above). Because McCarthy also fails to teach or suggest this feature (McCarthy discloses data cache unit 16 (Fig.2), which includes MMU 32, as part of the same processor 10 (Fig. 1)), Gaskins and McCarthy, taken alone or in combination, fail to teach or suggest all the features of Appellant's claim 25. Accordingly, Appellant respectfully requests the Board to overturn the §103 rejection based on the combination of Gaskins and McCarthy.

G. Claims 15, 16 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Armilli in view of McCarthy. Appellant respectfully submits a *prima facie* case of obviousness has not been presented at least because *Arimilli* and McCarthy, taken alone or in combination fail to teach or suggest *a table walk device connected to the memory controller and externally located from a memory management unit* as recited in Appellant's claim 14 (from which claims 15, 16 and 18 depend).

As discussed previously Arimilli fails to teach or suggest this feature (see paragraph C above). Further, McCarthy clearly teaches a table walk element within the MMU 32 (Figs. 2-3). Accordingly, McCarthy teaches away from Appellant's claims as well as being apparently incompatible with a device where a table walk element is allegedly separate from an MMU (e.g., Arimilli). Thus even assuming it would be proper to combine Arimilli with McCarthy (*arguendo*), Appellant respectfully submits the resultant combination fails to teach or suggest *a*

table walk device connected to the memory controller and externally located from a memory management unit as recited in Appellant's claims 15, 16 and 18 (by virtue of their dependency on claim 14). Since even in combination the cited references fail to teach or suggest all the features of Appellant's claims, *prima facie* obviousness is not established and the Board is respectfully requested to overturn the §103 rejection based on Arimilli and McCarthy.

H. Claims 19, 21 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli in view of Zolnowsky. The rejection relies on Arimilli to disclose all the features of these claims with the exception of the use of a table walk device adapted to receive memory access protection data, determine whether a process executing in the processor is permitted to access data stored in a memory device or abort a signal to the processor if the process is not permitted access to the memory device. The rejection relies on Zolnowsky to make up for these deficiencies.

Ignoring the properness of the motivation to combine these references, Appellant respectfully submits that Arimilli and Zolnowsky, taken alone or in combination, fail to teach or suggest *a table walk device connected to the memory controller and externally located from a memory management unit* as recited in Appellant's claim 14 (from which claims 19, 21 and 22 depend) as discussed previously (paragraph C above). Accordingly, *prima facie* obviousness is not established and the §103 rejection based on the combination of Arimilli and Zolnowsky is improper and Appellant respectfully requests the Board to overturn this rejection.

VIII. CONCLUSION.

It is respectfully submitted that in view of the foregoing all of the pending claims are patentable over the cited prior art references, alone or in any combination, and the Board is respectfully requested to overturn the rejections of record and allow this application to issue.

Respectfully submitted,

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Date: December 22, 2005

APPENDIX A
(Claims on Appeal)

Claims 1.-13. (Cancelled)

14. An apparatus, comprising:

a memory controller; and

a table walk device connected to the memory controller and externally located from a memory management unit (MMU).

15. The apparatus of claim 14, wherein the table walk device combines a portion of a virtual address and a portion of a base address.

16. The apparatus of claim 14, wherein the table walk device comprises a table base register to store a table base address.

17. The apparatus of claim 14, further comprising a translation lookaside buffer (TLB) coupled to the table walk device.

18. The apparatus of claim 17, wherein the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device.

19. The apparatus of claim 14, wherein the table walk device is adapted to receive memory access protection data.

20. The apparatus of claim 14, wherein the apparatus further comprises:

a processor coupled to the table walk device; and

a memory device coupled to the memory controller.

APPENDIX A
(Claims on Appeal)

21. The apparatus of claim 20, wherein the table walk device is adapted to determine whether a process executing in the processor is permitted to access data stored in the memory device.

22. The apparatus of claim 21, wherein the table walk device transmits an abort signal to the processor if the process is not permitted to access data stored in the memory device.

23. A system, comprising:

a processor;

a discrete memory controller adapted to perform a table walk operation and coupled to the processor; and

a volatile memory device coupled to the discrete memory controller.

24. The system of claim 23, further comprising a memory management unit (MMU), wherein the discrete memory controller is coupled to the processor via the MMU.

25. The system of claim 24, wherein the MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device.

26. The system of claim 23, wherein the discrete memory controller is adapted to provide address translation by using results of the table walk.

27. The system of claim 23, wherein the discrete memory controller performs a table walk by combining a portion of a virtual address and a portion of a base address to generate an address of a descriptor.

APPENDIX A
(Claims on Appeal)

28. The system of claim 23, wherein the volatile memory device is a dynamic random access memory (DRAM) device.

Claims 29.-33. (Cancelled)